AF

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/802,356
Filing Date	March 8, 2001
First Named Inventor	Hidekazu Watanabe
Art Unit	2112
Examiner Name	Jeremy S. Cerullo
Total Number of Pages in This Submission	22
Attorney Docket Number	80398P346

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) *(please identify below):*

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Thinh V. Nguyen, Reg. No. 42,034 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	December 12, 2005

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	**Tu T. Nguyen**		
Signature		Date	**December 12, 2005**

Based on PTO/SB/21 (09-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 11/30/2005.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
Application Number	09/802,356
Filing Date	March 8, 2001
First Named Inventor	Hidekazu Watanabe
Examiner Name	Jeremy S. Cerullo
Art Unit	2112
Attorney Docket No.	80398P346

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
☐ Charge fee(s) indicated below, except for the filing fee
☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.
☒ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify) _____					
				SUBTOTAL (2)	($) 500.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Thinh V. Nguyen	Registration No. (Attorney/Agent)	42,034	Telephone	(714) 557-3800
Signature				Date	12/12/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	09/802,356	Confirmation No. 7422
Applicant	:	Hidekazu Watanabe	
Filed	:	03/08/2001	
TC/A.U.	:	2112	
Examiner	:	Jeremy S. Cerullo	
Docket No.	:	080398.P346	
Customer No.	:	8791	

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant submits the following Appeal Brief pursuant to 37 C.F.R. § 41.37 for consideration by the Board of Patent Appeals and Interferences. Applicant also submits herewith our check number 203 in the amount of $500.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §41.20(b). Please charge any additional fees or credit any overpayment to our deposit Account No. 02-2666. A duplicate copy of the Fee Transmittal is enclosed for this purpose.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Sony Corporation and Sony Pictures Entertainment, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellants, the appellants' legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-30 of the present application are pending and remain rejected. The Applicant hereby appeals the rejection of claims 1-30.

IV. STATUS OF AMENDMENTS

The Applicants filed an amendment on September 8, 2005, in response to a Final Office Action issued by the Examiner on July 12, 2005. In response to the September 8, 2005 amendment, the Examiner issued an Advisory Action on September 27, 2005. The Applicants filed a Notice of Appeal from the Advisory Action on October 10, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

1. Independent claims 1, 11, and 21:

A system 100 includes, among others, N processors 110_1 to 110_N, N master buses 115_1 to 115_N, a master bus interface circuit 120, and K slave buses 135_1 to 135_K, slave devices 140_{jk} (j=1, . . .,K, k = 1,...,L, 1,. . . M, 1,. . ., P)[1]. The master bus interface circuit 120 includes K bus controllers 130_1 to 130_K. Each of the K bus controllers 130_1 to 130_K is connected to the N processors 110_1 to 110_N via the N master buses 115_1 to 115_N , respectively, and each of the corresponding K slave buses 135_1 to 135_K[2].

[1] See specification, page 3, paragraph [0013]; Figure 1.
[2] See specification, pages 3-4, paragraph [0015]; Figure 1 (element 120).

The bus controller 130 includes a bus arbiter 310, a write multiplexer 320, an address decoder 330, a read multiplexer 340, and a de-multiplexer 350[3].

The bus arbiter 310 is connected to the N processors 110_1 to 110_N via the N master buses 115_1 to 115_N. The bus arbiter 310 generates an arbitration select signal 315 based on result of arbitrating bus access information from the N processors 110_1 to 110_N[4].

The write multiplexer 320 is used to transfer the device access information from the selected processor to the destination slave device. The N inputs of the write multiplexer 320 are connected to the N master buses 115_1 to 115_N. The output of the write multiplexer is connected to one of the slave buses 135_1 to 135_K. Each of the bus controllers 130_1 to 130_K is assigned to each of the slave buses 135_1 and 135_K. The arbitration select signal 315 selects the bus access information from the processor that wins in the arbitration. The selected device access information is then transferred to the corresponding slave bus and directed to the destination slave device connected to that slave bus. The device access information includes information relating to the device access such as the device request, the slave address and the data to be written to the slave device[5].

2. Dependent claims 3, 13, and 23:

The address decoder 330 is connected to the bus arbiter 310 and the write multiplexer 320 to decode the slave address as provided by the device access information from the write multiplexer 320. The decoded slave address specifies the destination slave device. The address decoder 330 generates a number of device select signals, one of which is active to correspond to the destination slave device. The address decoder 330 also generates a device select signal 335 based on the specified slave address. The device select signal 335 is used to select device response information from the read multiplexer 340[6].

3. Dependent claims 4-5 and 7-10, 14-15 and 17-20, and 24-25 and 27-30:

The read multiplexer 340 is connected to the designated slave bus to provide bus response information from the device response information using the device select signal

[3] See specification, page 7, paragraph [0028]; Figure 3 (elements 310, 320, 330, 340 and 350).
[4] See specification, page 7, paragraph [0029].
[5] See specification, pages 7-8, paragraph [0030].
[6] See specification, page 8, paragraph [0031].

335. The device response information includes a device ready signal and the read data provided by the specified slave device[7].

The de-multiplexer 350 is connected to the read multiplexer 340 and the N processors 110_1 to 110_N to transfer the bus response information from the read multiplexer 340 to the processor that wins the arbitration as provided by the arbitration select signal 315 from the arbiter 310[8].

Examples of the processors 110_1 to 110_N include microprocessors, direct memory access (DMA) controllers, etc[9]. Examples of a slave include memory devices, peripheral devices. The K slave buses 135_1 to 135_K may be homogeneous or heterogeneous, i.e., there may be a set of slave buses of the same type and other sets of slave buses of different types, or all the slave buses are of the same type [10].

4. Dependent claims 6, 16, and 26:

The system 100 further includes a common memory interface 150 and a common memory 160[11]. The common memory interface 150 is connected to the K slave buses 135_1 to 135_K and the common memory 160 to allow any of the N processors 110_1 to 110_N, or even any of the slave devices 140_{jk} (j = 1, . . .,K, k = 1,...,L, 1,. . . M, 1,. . ., K) to access the common memory 160[12].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-2, 11-12, and 21-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,698,753 issued to Hubbins et al. ("Hubbins").
2. Claims 3, 13, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins as applied to claims 1-2 above, and further in view of U.S. Patent No. 5,590,369 issued to Burgess et al. ("Burgess").

---

[7] See specification, page 8, paragraph [0032].
[8] See specification, page 8, paragraph [0033].
[9] See specification, page 3, paragraph [0014]; page 5, paragraph [0020].
[10] See specification, page 4, paragraph [0016].
[11] See specification, page 3, paragraph [0013]; Figure 1 (elements 150 and 160).
[12] See specification, page 4, paragraph [0017]; page 9; paragraph [0039]; Figure 4.

3. Claims 4-5 and 7-10, 14-15 and 17-20, and 24-25 and 27-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins and Burgess as applied to claim 3 above, and further in view of U.S. Patent No. 5,453,737 issued to Opoczynski ("Opoczynski").

4. Claims 6, 16, and 26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins, Burgess and Opoczynski as applied to claim 4-5 and 7-10 above, and further in view of U.S. Patent No. 5,717,8957 issued to Leedom et al. ("Leedom").

VII. ARGUMENTS

A. Claims 1-2, 11-12, and 21-22 Are Not Obvious over Hubbins.

In the Final Office Action, the Examiner rejected claims 1-30 under 35 U.S.C. §103(a). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004).* Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

1) Claims 1-2, 11-12, and 21-22:

Claims 1-2, 11-12, and 21-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,698,753 issued to Hubbins et al. ("Hubbins").

Hubbins discloses a multiprocessor interface device. The device has ports A and B connected respectively to the bus systems of processors A and B and the ports are connected to a multiplexer to a common memory (Hubbins, col. 3, lines 29-31). The device has mode pins to define 4 modes. In the master and slave mode, the devices may be employed in parallel to accommodate wider word length (Hubbins, col. 10, lines 5-23).

The Examiner states that Hubbins discloses a multiplexer coupled to the first and second processors and to a slave, in this case the memory (Final Office Action, page 6, lines 1-2, Paragraph No. 9). Applicants respectfully disagree.

First, as clearly shown in Figure 1 in Hubbins, the multiplexer is merely connected to ports A and B and a 256x8 RAM. Ports A and B are contained inside the device (Hubbins, col. 3, lines 60-65; Figure 2, elements 2, 3, and 1). Since the ports are inside the device, they cannot be master buses. A master bus should be outside of a device to provide interface access to a plurality of other processors.

Furthermore, the host interfaces at ports A and B in Hubbins device cannot operate as a bus master. A master bus is a bus that multiple masters are connected. Since each master is able to control the bus by virtue of issuing address and data, the master bus is inherently bi-directional. Here, Hubbins merely discloses a host interface that receives address information and acts like a slave device to the processor by virtue of occupying 8 register locations in the address space of the processor (Hubbins, col. 3, lines 39-41; Figure 2, host interfaces 2 and 3). Therefore, the host interfaces 2 and 3 are not master buses.

Second, there is no slave bus. The memory is connected directly to the multiplexer. As defined above in the Microsoft Press Computer Dictionary, a bus is shared by different parts of a system. Here, as clearly shown in Figure 2 of Hubbins, the connections between the multiplexers MUXes 18 and 21 are directly to the address lines and the data lines of the RAM device 1. No sharing is possible. The address and data lines between the MUXes 18 and 21 to the RAM 1 are not made available to the external world. Furthermore, since the RAM, the arbitration latch, and the host interfaces are all housed in a single device, it is impossible for another device to share the address and data lines between the MUXes 18 and 21 and the RAM. Accordingly, the connection between the MUX and the memory cannot be a slave bus.

Furthermore, a slave bus is defined in the specification as a bus capable of being connected by a plurality of slave devices (See specification, paragraph [0016]). Here, the RAM is the only device connected to the MUXes. Therefore, Hubbins does not disclose, suggest, or render obvious a multiplexer coupled to a slave bus.

The Examiner further states that while Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Final Office Action, page 6, Paragraph 9). Applicants respectfully disagree. Using

several devices in parallel does not mean that a plurality of slave buses exists. Arranging these devices in parallel merely expands the width of the word length, e.g., from D0 – D7 to D0 – D7, D8 – D15, and D16 – D23 (Hubbins, Figure 9).

In summary, Hubbins effectively teaches away from the invention because all the interface circuits are located internally to a device. The host interfaces to ports A and B are not master buses. There are no a plurality of slave buses. Even if there is a slave bus, the slave bus is not connected to a plurality of devices.

B. Claims 3, 13, and 23 Are Not Obvious Over Hubbins in view of Burgess.

Claims 3, 13, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins as applied to claims 1-2 above, and further in view of U.S. Patent No. 5,590,369 issued to Burgess et al. ("Burgess").

Hubbins is discussed above.

Burgess discloses a bus supporting a plurality of data transfer sizes and protocols. A peripheral bus (Pbus) is used for transferring data between a processor and various peripheral devices (also denoted slaves) (Burgess, col. 4, lines 47-51). A Pbus master controls the operation of the Pbus (Burgess, col. 4, lines 52-54). The address bus connects the Pbus master with a synchronous/ asynchronous address decoder (Burgess, col. 6, lines 19-21). This decoder pairs each slave device with a corresponding address selected line connected to the slave(s) involved in the data transfer (Burgess, col. 6, lines 25-28).

Hubbins and Burgess, taken alone or in combination, do not disclose, suggest, or render obvious an address decoder coupled to the bus arbiter and the first mutiplexer to decode the slave address. As discussed above, Hubbins does not disclose a first multiplexer coupled to first and second master buses and slave address. Burgess merely discloses an address decoder to pair each slave device with a corresponding address selected line, not to decode a slave address in a plurality of slave buses.

Furthermore, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01. Here, Hubbins discloses a single memory inside a device. Modifying the device to include the address decoder to access multiple devices as

provided by Burgess would render Hubbins device unsatisfactory because its intended purpose is to allow accessing to a single memory, not a plurality of memories (Hubbins, col. 3, lines 29-32).

C. Claims 4-5 and 7-10, 14-15 and 17-20, and 24-25 and 27-30 Are Not Obvious Over Hubbins and Burgess and further in view of Opoczynski.

Claims 4-5 and 7-10, 14-15 and 17-20, and 24-25 and 27-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins and Burgess as applied to claim 3 above, and further in view of U.S. Patent No. 5,453,737 issued to Opoczynski ("Opoczynski").

Hubbins and Burgess are discussed above.

Opoczynski discloses a control and communication apparatus. A master controller communicates with a plurality of slave subsystems (Opoczynski, col. 2, lines 25-27). A serial port is connected through a selector, which receives a select line from the controller processor and controls which of the line drivers/receivers circuits receive the serial port I/O stream (Opoczynski, col. 3, lines 65-67; col. 4, line 1).

Hubbins, Burgess, and Opoczynski, taken alone or in any combination, do not disclose, suggest, or render obvious (1) a second multiplexer coupled to the first slave bus to provide bus response information from device response information using the device select signal; and (2) a de-multiplexer coupled to the second multiplexer and the first and second master buses to transfer the bus response information to one of the first and second processors using the arbitration select signal. As discussed above, Hubbins does not disclose a first multiplexer coupled to first and second master buses and slave address. Burgess does not disclose an address decoder to decode slave address. Opoczynski merely discloses a selector to control which of the line drivers/receivers receives the serial port I/O stream. The serial port I/O stream is not the same as the bus response information from device response information. Furthermore, the selector is not connected to a first slave bus that is also connected to another multiplexer.

The Examiner states that Opoczynski teaches a selector (multiplexer) that selects data from multiple data buses for I/O, and the multiplexer 21 of Figure 2 of Hubbins, while labeled a multiplexer, actually performs as de-multiplexer (Final Office Action, Page 7, lines 1-4, Paragraph No. 12). Applicants respectfully disagree for the following reasons.

As discussed above, Opoczynski merely discloses a selector which controls which of the line drivers/receivers circuits receive the serial port I/O stream. In essence, it connects the serial port I/O stream from the serial port 44 to one of the drivers/receivers 48A and 48B. Therefore, it does not select a single output from multiple inputs and cannot function as a multiplexer. Furthermore, even if it may function as a multiplexer, it does not provide bus response information from device response information. It merely connects the serial port I/O stream to one of the drivers/receivers. The serial port I/O stream is not the bus response information. A serial port is not a bus.

Regarding the multiplexer 21 in Hubbins, even if this device function as a de-multiplexer, it merely transfers the data output of the RAM (Hubbins, col. 4, lines 36-38), not the bus response information from the device response information. The bus response information may include address, data, or device ready signal (See, for example, Specification, paragraph [0032], Figure 3).

D. Claims 6, 16, and 26 Are Not Obvious Over Hubbins, Burgess and Opoczynski and further in view of Leedom.

Claims 6, 16, and 26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins, Burgess and Opoczynski as applied to claim 4-5 and 7-10 above, and further in view of U.S. Patent No. 5,717,8957 issued to Leedom et al. ("Leedom").

Leedom discloses an associative scalar data cache with write-through capabilities for a vector processor. A scalar/vector supercomputer includes a scalar/vector processor connected through a common memory interface to one or more sections of common memories (Leedom, col. 5, lines 19-23).

Hubbins, Burgess, Opoczynski, and Leedom, taken alone or in any combination, do not disclose, suggest, or render obvious the plurality of slave buses being coupled to a common memory via a common memory interface. As discussed above, Hubbins, Burgess, and Opoczynski, individually or collectively, do not disclose first and second master buses, a plurality of slave buses, a multiplexer, an address decoder, a second multiplexer, and a de-multiplexer. Leedom merely discloses a common memory interface to a scalar/ vector processor. A scalar/ vector processor is not a slave device connected to a slave bus. The common memory interface in Leedom is connected directly to the V registers, the B and T registers, the address selector, and the instruction buffers (Leedom,

Figure 1), not to a plurality of slave buses. Since none of Hubbins, Burgess, and Opoczynski discloses or suggests master buses and a plurality of slave buses, and Leedom does not disclose or suggest a common memory interface coupled to a plurality of slave buses, the combination of these prior art references is improper.

In summary, the Examiner has not met the burden of establishing a prima facie case of obviousness in rejecting claims 1-30 under 35 U.S.C. §103(a). "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Furthermore, although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." In re Mills 916 F.2d at 682, 16 USPQ2d at 1432; In re Fitch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992). When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) The

claimed invention must be considered as a whole; (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) Reasonable expectation of success is the standard with which obviousness is determined. Hodosh v. Block Drug Col, Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). Here, none of the cited prior art references discloses or suggests the desirability of the combination. Furthermore, the Examiner has failed to present a convincing line of reasoning as to why the claimed invention is obvious in light of the teachings of Hubbins, Burgess, Opoczynski, and Leedom, either individually or in any combination.

Therefore, Applicants believe that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references.

VIII. CONCLUSION

Applicant respectfully requests that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are neither anticipated nor rendered obvious by the prior art.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: December 12, 2005

THINH V. NGUYEN
Reg. No. 42,034

12400 Wilshire Blvd., 7th Floor
Los Angeles, CA 90025-1026
(714) 557-3800

IX. CLAIMS APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (original) An apparatus comprising:

a bus arbiter coupled to first and second processors via first and second master buses, respectively, to generate an arbitration select signal based on result of arbitrating bus access information from the first and second processors; and

a first multiplexer coupled to the first and second master buses and a first slave bus in a plurality of slave buses to provide device access information selected from the bus access information using the arbitration select signal, the device access information being transferred to a first slave device connected to the first slave bus.

2. (original) The apparatus of claim 1 wherein the device access information includes at least one of slave address and write data.

3. (original) The apparatus of claim 2 further comprising:

an address decoder coupled to the bus arbiter and the first multiplexer to decode the slave address, the decoded slave address specifying the first slave device, the address decoder generating device select signal.

4. (original) The apparatus of claim 3 further comprising:

a second multiplexer coupled to the first slave bus to provide bus response information from device response information using the device select signal; and

a de-multiplexer coupled to the second multiplexer and the first and second master buses to transfer the bus response information to one of the first and second processors using the arbitration select signal.

5. (original) The apparatus of claim 4 wherein the device response information includes at least one of device ready status and read data.

6. (original) The apparatus of claim 5 wherein the plurality of slave buses are coupled to a common memory via a common memory interface.

7. (original) The apparatus of claim 5 wherein one of the first and second processors is a direct memory access (DMA) controller.

8. (original) The apparatus of claim 5 wherein one of the first and second processors is a microprocessor.

9. (original) The apparatus of claim 5 wherein the first slave device is one of a memory device and a peripheral device.

10. (original) The apparatus of claim 5 wherein the plurality of slave buses includes at least one of a homogenous set and a heterogeneous set.

11. (original) A method comprising:

generating an arbitration select signal based on result of arbitrating bus access information from first and second processors via first and second master buses, respectively; and

providing device access information selected from the bus access information using the arbitration select signal, the device access information being transferred to a first slave device connected to a first slave bus from a plurality of slave buses.

12. (original) The method of claim 11 wherein providing device access information comprises providing at least one of slave address and write data.

13. (original) The method of claim 12 further comprising:

decoding the slave address, the decoded slave address specifying the first slave device; and

generating device select signal.

14. (original) The method of claim 13 further comprising:

providing bus response information from device response information using the device select signal; and

transferring the bus response information to one of the first and second processors using the arbitration select signal.

15. (original) The method of claim 14 wherein providing the bus response information from device response information comprises providing the bus response information from at least one of device ready status and read data.

16. (original) The method of claim 15 further comprising accessing a common memory via a common memory interface.

17. (original) The method of claim 15 wherein one of the first and second processors is a direct memory access (DMA) controller.

18. (original) The method of claim 15 wherein one of the first and second processors is a microprocessor.

19. (original) The method of claim 15 wherein the first slave device is one of a memory device and a peripheral device.

20. (original) The method of claim 15 wherein the plurality of slave buses includes at least one of a homogenous set and a heterogeneous set.

21. (original) A system comprising:

first and second processors coupled to first and second master buses;

a plurality of slave buses, each of the slave buses coupled to a plurality of slave devices; and

a master bus interface circuit coupled to the first and second master buses and the plurality of slave buses, the master bus interface circuit comprising a plurality of bus controllers, each of the bus controllers comprising:

a bus arbiter coupled to the first and second processors via the first and second master buses, respectively, to generate an arbitration select signal based on result of arbitrating bus access information from the first and second processors, and

a first multiplexer coupled to the first and second master buses and a first slave bus in the plurality of slave buses to provide device access information selected from the bus access information using the arbitration select signal, the device access information being transferred to a first slave device connected to the first slave bus.

22. (original) The system of claim 21 wherein the device access information includes at least one of slave address and write data.

23. (original) The system of claim 22 wherein each of the bus controllers further comprising:

an address decoder coupled to the bus arbiter and the first multiplexer to decode the slave address, the decoded slave address specifying the first slave device, the address decoder generating device select signal.

24. (original) The system of claim 23 wherein each of the bus controllers further comprising:

a second multiplexer coupled to the first slave bus to provide bus response information from device response information using the device select signal; and

a de-multiplexer coupled to the second multiplexer and the first and second master buses to transfer the bus response information to one of the first and second processors using the arbitration select signal.

25. (original) The system of claim 24 wherein the device response information includes at least one of device ready status and read data.

26. (original) The system of claim 25 further comprising:

a common memory coupled to the plurality of slave buses via a common memory interface to provide access to one of the first and second processors.

27. (original) The system of claim 25 wherein one of the first and second processors is a direct memory access (DMA) controller.

28. (original) The system of claim 25 wherein one of the first and second processors is a microprocessor.

29. (original) The system of claim 25 wherein the first slave device is one of a memory device and a peripheral device.

30. (previously presented) The system of claim 25 wherein the plurality of slave buses includes at least one of a homogenous set and a heterogeneous set.

XI. EVIDENCE APPENDIX

None

XII. RELATED PROCEEDINGS APPENDIX

None